

REMARKS

Claims 1-20 remain pending in the present application. Claims 1-3 have been amended. Accordingly, claims 1-20 are presented to the Examiner for re-examination in light of the amendments and remarks made herein.

In PTO form 948 (i.e., the Notice of Draftperson's Patent Drawing Review), the Draftperson objected to the Figures for various informalities. In response thereto, Applicant submits new formal drawings (Figures 1-8 on five sheets) that are attached hereto for consideration by the Draftperson.

The Examiner objected to the specification because there is some missing text caused by holes that were punched at the top of the pages of the specification. In response thereto, Applicant submits a substitute specification, which is a photocopy of the specification as originally filed on December 20, 1999. The photocopy specification that is attached hereto does not contain any new matter.

The Examiner rejected claims 1-3 under 35 U.S.C. §102(a) as being anticipated by Ker (U.S. Patent No. 5,901,022). Applicants respectfully traverse this rejection.

In the rejection, the Examiner alleges that Ker discloses an ESD circuit having an inductor connected to an ESD clamp device. The Examiner further alleges that Ker discloses in Figures 11 and 12 that the inductor is formed on a substrate (die). Applicant, however, respectfully disagrees with the Examiner's interpretation of Ker. Although Ker may disclose an electrostatic discharge (ESD) protection circuit, it is noted that the invention of Ker (in the various embodiments illustrated in Figures 9-12) includes a single coil and a single ESD clamp

device. It is respectfully submitted, however, that independent claim 1 of the present invention (as amended) recites “an inductor having a plurality of turns in the shape of a coil” and “a plurality of electrostatic discharge (ESD) clamp devices.” Applicant respectfully submits that the ESD circuit of Ker has an inductor coupled to a single ESD clamp device and that there is absolutely no teaching or suggestion provided by Ker to provide more than one ESD clamp device as defined by claim 1 of the present invention. Accordingly, because Ker fails to teach providing a plurality of ESD clamp devices in an ESD protection network, Ker cannot possibly anticipate claim 1 of the present invention (as amended), and claims 2 and 3 that depend thereon.

The Examiner further rejected claim 1 under 35 U.S.C. §102(a) as being anticipated by Japanese Patent Abstract JP-67486 (hereinafter “the Japanese reference”). Applicants respectfully traverse this rejection.

Although the Japanese reference cited by the Examiner may disclose an ESD protection circuit, Applicant respectfully submits that the reference fails to teach or suggest using more than one ESD clamp device for the protection circuit. As previously mentioned, claim 1 of the present invention (as amended) includes a plurality of ESD clamp devices. Accordingly, because the Japanese reference fails to teach the use of more than one ESD clamp device within an ESD protection network, it is respectfully submitted that the Examiner’s allegation that the Japanese reference anticipates claim 1 of the present invention is improper.

The Examiner rejected claims 2 and 3 under 35 U.S.C. §103(a) as being unpatentable under Japanese Patent Abstract (JP-67486) in view of Ker. Applicants respectfully traverse this rejection.

In the rejection, the Examiner alleges that the Japanese reference discloses all the features of claim 1 except the inductor being fabricated on a substrate or an IC die. The Examiner relies on Ker for teaching (in Figures 11 and 12) an inductor being formed on a substrate/die (bond metal pad) to avoid increasing the total layout area of the protection circuit. The Examiner then alleges that it would have been obvious to utilize the teaching of Ker to form the inductor on the bond pad to save space on the integrated circuit. Applicant, however, respectfully disagrees with this rejection.

As previously indicated, although the Japanese reference cited by the Examiner may disclose an ESD protection circuit, the reference fails to teach or suggest using more than one ESD clamp device for the protection circuit. Claim 1 of the present invention (as amended) includes a plurality of ESD clamp devices. Accordingly, because the Japanese reference fails to teach the use of more than one ESD clamp device within an ESD protection network, it is respectfully submitted that claims 2 and 3 of the present invention are distinct therefrom. Additionally, although Ker may teach an inductor being formed on a substrate as alleged by the Examiner, Applicant respectfully submits that the ESD circuit of Ker has an inductor coupled to a single ESD clamp device and that there is absolutely no teaching or suggestion provided by Ker to provide more than one ESD clamp. Accordingly, because neither the Japanese reference nor Ker teach to provide a plurality of ESD clamp devices in an ESD protection network, these references cannot possibly make obvious claims 2 and 3 of the present invention.

The Examiner also rejected claims 4-20 under 35 U.S.C. §103(a) as being unpatentable under Ker in view of Lee (U.S. Patent No. 5,831,331). Applicants respectfully traverse this rejection.

In the rejection, the Examiner alleges that Ker discloses an ESD protection circuit connected to an inductor formed on a substrate of an integrated circuit, but fails to disclose the physical structure of the multi-coil turn inductor on a plurality of insulating layers. The Examiner alleges that Lee discloses an integrated circuit inductor having multiple coil turns. The Examiner then alleges that it would have been obvious to utilize the inductive structure taught by Lee in Ker to save space on the integrated circuit and for ease of manufacturing. Applicant respectfully disagrees with this rejection.


The Lee reference is directed to an inductor having multiple turns disposed one above another in respective metallization layers of an IC. Although Lee may teach or suggest a “stacked” coil configuration, Lee does not teach or suggest the use of more than one ESD clamp device with the plurality of coils. It is respectfully submitted that a combination of Ker with Lee would teach at most an ESD protection circuit having a plurality of coils stacked upon one another with a single ESD clamp device. Accordingly, it is submitted that Ker and Lee, taken alone or in combination, do not teach or suggest the use of more than one ESD clamp device as set forth in independent claims 4 and 18 of the present invention. For example, claim 4 recites “*a plurality of electrostatic discharge (ESD) clamp devices,*” and claim 18 recites “*providing a plurality of electrostatic discharge (ESD) clamp devices*” (emphasis added). Therefore, because the Ker or Lee references, either taken alone or in combination, fail to teach or suggest providing more than one ESD clamp device for use with a plurality of coils, it is respectfully submitted that the Examiner’s allegation of obviousness in view of the Ker and Lee references is improper.

Applicants respectfully submit that the remaining rejections in the present application are improper and should be withdrawn because the cited references fail to teach or suggest all of the limitations of the claims as discussed in detail above. Accordingly, in view of the amendments and remarks presented herein, a Notice of Allowance is respectfully solicited.

It is believed that no fee is due in connection with filing this paper; however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason, the Assistant Commissioner is authorized to deduct said fees from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.065900.

The Examiner is invited to contact the undersigned at (713) 934-4058 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,



George J. Oehling
Reg. No. 40,471

WILLIAMS, MORGAN & AMERSON
7676 Hillmont, Suite 250
Houston, Texas 77040
(713) 934-7000

Date: 4/30/02



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APPENDIX A

1. (Amended) An electrostatic discharge (ESD) protection network, comprising:
an inductor having a plurality of [at least one] turns in the shape of a coil, the [at least one] plurality of turns having an inductance; and
~~[at least one]~~ a plurality of electrostatic discharge (ESD) clamp devices, each one of said plurality of ESD clamp devices having a parasitic capacitance, said plurality of ESD clamp devices connected to the [at least one] turns of said inductor, the inductance of said [at least one] turns and the parasitic capacitance of said [at least one] ESD clamp devices thereby forming a low pass filter.
2. (Amended) The ESD protection network of claim 1, wherein said [at least one turn] plurality of turns and said [at least one] plurality of ESD clamp devices are fabricated on a surface selected from the group consisting of a substrate and an integrated circuit die.
3. (Amended) The ESD protection network of claim 1, wherein said [at least one] plurality of turns and said [at least one] plurality of ESD clamp devices are fabricated on an integrated circuit die.

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